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**Question Paper Code : 11323**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2012.

Third Semester

Electronics and Communication Engineering

EC 2203/147302/EC 34/10144 EC 304/080290010 – DIGITAL ELECTRONICS

(Regulation 2008)

(Common to PTEC 2203 – Digital Electronics for Third Semester B.E. (Part-Time)  
Electronics and Communication Engineering – Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the given Boolean expression  $F = x' + xy + xz' + xy'z'$ .
2. Implement the given function using NAND gates  $F(x, y, z) = \Sigma m(0, 6)$ .
3. Draw the logic diagram of a serial adder.
4. Design a three bit even parity generator.
5. How a D flipflop is converted into T flipflop.
6. Design a 3 bit ring counter and find the mod of the designed counter.
7. How the memories are classified?
8. Draw the logic diagram of static RAM cell and Bipolar RAM cell.
9. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
10. Design a 3 input AND gate using verilog.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the given Boolean function using tabulation method  
 $F(A, B, C, D) = \Sigma m(1, 2, 3, 5, 7, 9, 10, 11, 13, 15)$ .

Or

- (b) Draw the circuit diagram of a two input TTL NAND gate with tristate output and explain its action, clearly showing logic and voltage levels.

12. (a) Design a four bit BCD to excess-3 code converter. Draw the logic diagram.

Or

- (b) (i) Design a 4 bit parallel adder/subtractor and draw the logic diagram. (8)

- (ii) Draw the logic diagram of a BCD adder and explain its operation. (8)

13. (a) Design a sequence detector which detects the sequence "01110" using D flipflops (one bit overlapping).

Or

- (b) (i) Design a 4 bit bi-directional shift register. (8)

- (ii) Design a 3 bit Johnson counter and explain its operation. (8)

14. (a) (i) Implement a 3 bit up/down counter using PAL devices.  
(ii) Implement binary to Gray code converter using PROM devices. (8 + 8)

Or

- (b) Write short notes on :

- (i) Memory decoding. (8)

- (ii) Memory expansion. (8)

15. (a) Design the following circuits using verilog

- (i) 4 to 1 multiplexer (8)

- (ii) 2 bit up/down counter. (8)

Or

- (b) Write short notes on races and hazards that occur in asynchronous circuits. Discuss a method used for race free assignment with example.